REMARKS

Favorable reconsideration of this application in view of the remarks to follow is respectfully requested. Since the present Response raises no new issues, and in any event, places the application in better condition for consideration on appeal, entry thereof is respectfully requested under the provisions of 37 C.F.R. §1.116.

Further search is not required for consideration of amended Claims 23 and 40 as the limitations added are a property of the SiGe interlayer incorporated in the originally submitted claims and therefore previous searches relating to the SiGe interlayer are applicable to amended Claims 23 and 40. Since the above amendments do not introduce any new matter into the application, entry thereof is respectfully requested.

Before addressing the specific grounds of rejection raised in the present Office Action, applicants have canceled Claim 41 without prejudice or disclaimer; and amended Claims 23 and 40.

Claim 23 has been amended to recite that the *SiGe interlayer has a thickness of less than about 3.0 nm.* Support for this amendment is found in FIG. 4 of applicants' specification. FIG. 4 depicts a TEM of applicants' disilicide film formed from a metal alloy having 2.1% Ge, where the Ge diffuses to the interface between the disilicide film and the substrate to form a SiGe interlayer. Referring to FIG. 4, the SiGe interlayer is the darker region at the interface, referenced by point A, separating the dislicide layer from the underlying substrate. Measuring the SiGe interlayer using the supplied 30.0 nm scale bar indicates that the SiGe interlayer has a thickness of less than 3.0 nm. Referring to Page 17, paragraph 2, applicants disclose that the 3.0 nm probe size is thicker than the SiGe interlayer further supporting that the SiGe interlayer has a thickness of less than about 3.0 nm.

Claim 40 has been amended to more clearly and positively recite applicants' claimed structure having a Si-Ge interlayer *positioned on an interface between a first disilicide layer and a substrate, wherein the Si-Ge interlayer does not substantially extend beyond the interface.* Support for this amendment is found in applicants' specification on Page 11, paragraph 2, where applicants' disclose that:

> "It is noted that during an annealing step of the present invention the Ge diffuses to the interface formed between the substrate and the metal germanium alloy layer. To form the silicide layer and the Si-Ge interlayer in the structure, annealing is carried out using a rapid thermal anneal (RTA) process using a gas atmosphere, e.g., He, Ar, Ne or forming gas, at a temperature of from about 400°C to about 700°C for a time period of about 300 seconds or less."

Referring to FIG 4. depicting a TEM of a SiGe interlayer formed using anneal conditions similar to those disclosed in the above passage, a SiGe interlayer having a thickness of less than 3.0 nm is formed at the interface between the metal disilicide and the substrate. Therefore. FIG. 4 indicates that the SiGe interlayer does not substantially extend beyond the interface between the metal disilicide and the underlying substrate on which the SiGe interlayer is formed.

In the present Office Action, Claim 40 stands rejected under 35 U.S.C. §112, first paragraph, for allegedly failing to describe the subject matter of the present invention in such a way to enable one skilled in the art to which it pertains to make and/or use the invention. Claims 23, 25-28, 31-39, and 41 stand rejected under 35 U.S.C. §112, first paragraph, as allegedly failing to comply with the enablement requirement. Claims 23, 25-27, 36, 40 and 41 stand rejected as allegedly unpatentable over U.S. Patent No. 5,710,450 to Chau, et al. ("Chau, et al.") in view of U.S. Patent No. 5,830,775 to Maa, et al. ("Maa, et al."). Claim 28 stands rejected, under 35 U.S.C. §103(a), as allegedly unpatentable over the combination of Chau, et al., Maa, et al. and U.S. Patent No. 5,510,295 to Cabral Jr., et al. ("Cabral Jr., et al.").

Referring to the §112 rejection of Claim 40, it is the Examiner's position that applicants fail to disclose the structural features of an electrical contact, where the electrical contact has a SiGe interlayer, which does not substantially extend beyond the edges of a metal disilicide. In light of the current amendment to Claim 40, applicants respectfully disagree and submit the following.

The test of enablement is whether one reasonably skilled in the art could make or use the invention with information known in the art without undue experimentation. *United States v. Telectronics, Inc.*, 857 F.2d 778, 785, 8 USPQ2d 1217, 1223 (Fed. Cir. 1988). First, it is known within the art that metal silicide regions are electrical contact regions for semiconducting devices. Second, FIGS. 1(a)-(f) illustrate a method of making the inventive silicide structure. Third, the originally filed specification describes how a SiGe interlayer is formed at that interface between the silicide and the Si substrate in a manner, which would enable one of ordinary skill in the art to make the inventive electrical contact.

Applicants observe that refractory silicides are known within the semiconductor art as electrical contacts. "Refractory metal silicides are important in wafer fabrication because of the need to reduce the electrical resistance of the many silicon contacts in the source/drain and gate region for chip performance." Michael Quirk, *Semiconductor Manufacturing Technology*, Prentice Hall Inc., pg. 309 (2001)(ISBN 0-13-081520-9). The specification need not disclose what is well known to those skilled in the art and already available to the public. *In re Buchner*, 929 F.2d 660, 661; 18 USPQ2d 1331, 1332 (Fed. Cir. 1991). Additionally, referring to Page 14 paragraph 3 of the originally filed specification, applicants have defined the structure of the inventive electrical contact to include a substrate 10 of a silicon-containing material and a first layer of a metal disilicide 24, where the substrate 10 and the metal disilicide are separated by a

SiGe interlayer 22, as depicted in FIG. 1F and as recited in Claim 40. Applicants may define in the claims what they regard as their invention, essentially in whatever terms they choose, so long as the terms are not used in ways that are contrary to the accepted meaning in the art. *See In re Swinehart,* 439 F.2d 210, 160, USPQ 226 (CCPA 1971). Therefore, since it is known within the art that silicides are electrical contacts and since the claimed electrical contact is described in a manner consistent with the meaning of the art the applicants have provided an electrical contact for the purposes of 35 U.S.C. §112, paragraph 1.

Applicants further submit that FIGS. 1(a) – 1(f) depict a silicide structure, known within the art as an electrical contact, and is not merely an order of layers in cross-section, as alleged by the Examiner. Applicants disclose, referring to Page 7 paragraph 2, that FIGS. 1(a)-1(f) illustrate the basic processing steps of the present invention, which utilizes a metal Ge alloy as the silicide starting material. As discussed above, it is known within the art that silicides function as the electrical contacts to semiconducting materials.

Applicants further disclose how the SiGe interlayer is formed at the interface between the silicide and the Si substrate in a manner that would enable one of ordinary skill in the art to make the inventive electrical contact. Referring to Page 11 paragraph 2, applicants disclose where a structure is annealed so as to form a metal silicide layer and a Si-Ge interlayer; where the interlayer separates the silicide from the substrate. Applicants further disclose, "that during this annealing step of the present invention the Ge diffuses to the interface formed between the substrate and the metal alloy layer." Additionally, FIG. 1C depicts where the SiGe interlayer 22 is formed between the metal silicide layer 20 and the substrate10.

Finally, applicants disclose annealing parameters that would produce the inventive SiGe interlayer positioned on an interface between the metal disilicide and the underlying Si substrate,

where the SiGe interlayer does not substantially extend beyond the interface. Referring to Page 12, paragraph 2, applicants disclose that, "to form the silicide layer and the Si-Ge interlayer in the structure, annealing is carried out using a rapid thermal anneal process using a gas atmosphere, e.g., He, Ar, Ne or forming gas, at a temperature of about 400°C to about 700°C for a time period of about 300 seconds or less using a continuous heating regime or a ramp and soak heating regime." The disclosed annealing temperature range provides enough thermal energy to produce the SiGe interlayer by diffusing Ge to the interface between the metal silicide and the substrate; but does not provide enough energy to diffuse Ge uniformly into the substrate in a manner that would produce a SiGe interlayer that substantially extends beyond the interface. Applicants note that although some Ge diffuses into the substrate, the disclosed annealing process allows for the formation of a SiGe interlayer that does not substantially extend beyond the metal disilicide/Si substrate interface on which it the SiGe interlayer was formed. As discussed above, FIG. 4 clearly depicts the results of applicants' process that forms a SiGe interlayer at the metal disilicide/Si substrate interface, in which the SiGe interlayer has a thickness of less than about 3.0 nm clearly indicating that the SiGe interlayer does not substantially extend beyond the interface on which it was formed.

Applicants submit that the interface between the metal silicide and the substrate is known in the art to include both a vertical (sidewall interface) and a horizontal (base interface) dimension. Applicants have enabled one of ordinary skill in the art to produce the inventive SiGe layer, where the SiGe interlayer does not substantially extend beyond the metal disilicide/Si substrate interface at which the SiGe interlayer was formed. The disclosed annealing temperatures do not cause the Ge to substantially diffuse beyond the interface of the metal disilicide and the Si substrate in both the horizontal and vertical direction. Applicants submit

that although some Ge diffuses into the substrate, applicants' process does not provide enough thermal energy for the Ge to uniformly diffuse into the substrate and cause the SiGe interlayer to substantially extend beyond the metal alloy/Si substrate interface. Instead, applicants' disclosed annealing process causes the Ge from the metal alloy layer, in which the Ge was originally deposited, to diffuse to the metal alloy/Si substrate interface, forming the SiGe interlayer.

In further support of applicants' position, a Declaration under 37 C.F.R. § 1.132 is provided in which Mr. Lavoie, an originally named inventor, attests to the aforementioned facts.

Based on the above amendments and remarks, the §112 rejection has been obviated; therefore reconsideration and withdrawal of the instant rejection to Claim 40 is respectfully requested.

Turning now to the rejection of Claims 23, 25-28, 31-39 and 41 under 35 U.S.C. §112, first paragraph, applicants respectfully submit that the current amendment to Claim 23 overcomes the instant rejection. It is the Examiner's position that the concentration of Ge in the SiGe interlayer recited in amended Claim 23 was not supported by the specification. In response to the Examiners' comments and for the purposes of advancing prosecution, applicants have removed the Ge concentrations from Claim 23. Applicants have also cancelled Claim 41, without prejudice or disclaimer. In light of the current amendment to Claim 23, the instant §112 rejection has been obviated; therefore applicants respectfully request that the rejection be withdrawn.

Turning to the rejection of Claims 40 under 35 U.S.C. § 103(a), applicants submit that the applied prior art fails to teach or suggest an electrical contact including a first layer of metal disilicide, wherein said metal of said disilicide is selected from the group consisting of Ti, Co and mixtures thereof, and said exposed region of said substrate and said first layer are separated

by a *Si-Ge interlayer positioned on an interface between a first metal disilicide layer and a substrate, wherein said Si-Ge interlayer does not substantially extend beyond said interface*, as recited in amended Claim 40.

Chau, et al., referring to FIGS. 3C to 3D, disclose depositing a SiGe semiconducting layer 314 atop a substrate; forming spacers 318 atop a portion of the SiGe semiconducting layer 314; and then forming silicide regions 320 atop the SiGe semiconducting layer 314, where the portion of the SiGe semiconducting layer 314 underlying the spacers 318 substantially extends beyond the silicide region 320. Referring to Column 7, lines 1-7, Chau, et al. disclose that the spacers 318 have a thickness ranging from 50.0 nm to 250.0 nm. Therefore, the portion of the SiGe layer 314 underlying the spacers 318 extends from approximately 50.0 nm to approximately 250.0 nm from the overlying silicide regions 320.

The inventive structure includes a SiGe interlayer that does not substantially extend from the metal disilicide/Si substrate interface at which the SiGe interlayer was formed. Referring to FIG. 4, it is clear that applicants' SiGe interlayer is formed having a thickness of less than approximately 3.0 nm at the interface between the metal disilicide and the Si substrate. As discussed above, it is well known within the art that an interface has both a vertical and lateral dimension. The structure disclosed in Chau, et al. (see FIG. 3F) includes a 50.0 nm to 250.0 nm portion of the SiGe semiconducting layer 314 positioned underlying spacer 318 and substantially extends away from the overlying silicide 320. Therefore, Chau, et al. fail to teach or suggest an electrical contact structure including a *Si-Ge interlayer positioned on an interface between the first metal disilicide layer and the substrate, wherein the Si-Ge interlayer does not substantially extend beyond said interface*, as recited in amended Claim 40.

Additionally, applicants submit that one of ordinary skill in the art could not modify Chau, et al. in a manner to produce the claimed structure, since Chau, et al. teach away from forming a *Si-Ge interlayer positioned on an interface between a first metal disilicide layer and a substrate, where the Si-Ge interlayer does not substantially extend beyond the interface.* A prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. *W.L. Gore and Associates, Inc. v. Garlock, Inc.,* 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983).

Chau, et al. disclose, referring to Column 6, lines 35-40, that a solid-state diffusion step occurs directly after the formation of semiconductor material 314 with a rapid thermal process (RTP) at a temperature between 800°C to 1000°C for 5 to 60 seconds in a nitrogen N_2 ambient. The temperature range disclosed in Chau, et al. is greater than applicants' annealing temperature range, which includes temperatures of less than about 700°C. Chau, et al. disclose that during the solid-state diffusion step, dopants (Ge) are able to easily diffuse in a single direction (laterally) below the first sidewall spacer 310 and underneath the outside edge of polysilicon gate electrode 306. Chau, et al. further disclose, referring to Column 6, lines 50-58, that the lateral diffusion results in an ultra shallow tip 317, which is characterized by a very sharp and abrupt junction with the substrate 300 and that an abrupt junction improves the punch-through characteristics of the fabricated transistor. Therefore Chau, et al. teach that it is advantageous to promote lateral diffusion of Ge away from the interface of the overlying silicide 320.

Further, Chau, et al. teach away from reducing the width of spacer 318, and hence reducing the portion of the SiGe semiconducting layer 314 extending away from silicide region 320, because the spacer 318 "must be formed thick and wide enough to provide a sufficient mask to prevent the deep, high dose ion implantation of the source/drain contact regions from

overwhelming the fabricated tip region 321." Therefore, since Chau, et al. teach that it is advantageous to promote the lateral spread of the Ge from the SiGe semiconducting layer 314 to produce the ultra shallow tip 317 and then producing wide spacers 318 over a substantial portion of SiGe semiconducting layer 314 to produce source/drain contact regions that do not overwhelm the fabricated tip region 321, followed by the formation of the silicide region 320 flanking the wide spacers 318; Chau, et al. lead away from the applicants claimed electrical contact having a *Si-Ge interlayer positioned on an interface between said first layer and said substrate, wherein said Si-Ge interlayer does not substantially extend beyond said interface*, as recited in amended Claim 40.

Maa, et al. provide a raised source/drain electrode structure including a metal disilicide layer. Maa, et al. do not teach or suggest forming a SiGe interlayer between the metal disilicide and the substrate. Therefore, Maa, et al. fail to teach or suggest the applicants' claimed electrical contact including a *Si-Ge interlayer positioned on an interface between said first layer and said substrate, wherein said Si-Ge interlayer does not substantially extend beyond said interface*, as recited in amended Claim 40.

Cabral Jr., et al. provide a method of forming a silicide where a precursory metal 16 is deposited atop a refractory metal 14 atop a Si substrate 10, where a silicide is formed following anneal process steps. Cabral Jr., et al. do not teach or suggest forming a SiGe interlayer between the metal disilicide and the substrate. Therefore, Cabral Jr., et al. fail to teach or suggest the applicants' claimed electrical contact including a *Si-Ge interlayer positioned on an interface between said first layer and said substrate, wherein said Si-Ge interlayer does not substantially extend beyond said interface*, as recited in amended Claim 40.

Now referring to the §103 rejections of Claims 23, 25-28, 31 and 36, applicants respectfully submit that the applied references fail to teach or suggest all of the claimed limitations of applicants' electrical contact, as recited in amended Claim 23. Applicants have amended Claim 23 to recite an electrical contact having a first layer of metal disilicide which includes an additive or Ge, wherein said metal of said disilicide is selected from the group consisting of Ti, Co and mixtures thereof, and said exposed region of said substrate and said first layer are separated by a Si-Ge interlayer, *wherein said Si-Ge interlayer has a thickness less than about 3.0 nm.*

Applicants submit that the applied prior art references fail to teach or suggest an electrical contact including a *Si-Ge interlayer having a thickness less than about 3.0 nm*, as recited in amended Claim 23. "To establish a prima facie case of obviousness of a claimed invention all the claimed limitations must be taught or suggested by the prior art" *In re Wilson,* 424 F.2d 1382, 1385, 165 USPQ 44, 496 (CCPA 1970).

Chau, et al. disclose, referring to Column 5, lines 29-31, a SiGe alloy layer 314 having a thickness of between 200 Å (20.0 nm) – 2000 Å (200.0 nm), with approximately 600 Å (60.0 nm) being preferred. Therefore, Chau, et al. fail to teach or suggest a SiGe interlayer having *a thickness less than about 3.0 nm*, as recited in amended Claim 23.

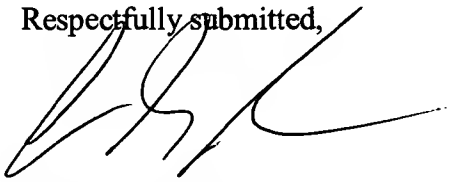
The applied secondary references fail to fulfill the deficiencies of Chau, et al. since the applied secondary references also fail to teach or suggest the applicants' claimed electrical contact including a SiGe interlayer having *a thickness less than about 3.0 nm.* As discussed above, the applied secondary references, Maa, et al. and Cabral Jr., et al., fail to teach or suggest an electrical contact having a SiGe interlayer. Therefore, the applied secondary references fail to

teach or suggest an electrical contact including a SiGe interlayer having *a thickness less than about 3.0 nm*, as recited in amended Claim 23.

Based on the above amendments and remarks, the §103 rejections have been obviated; therefore reconsideration and withdrawal of the instant rejection are respectfully requested.

Wherefore, reconsideration and allowance of the claims of the present application are respectfully requested.

Respectfully submitted,



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